



BBG-520

Six Channel Digital-to-Synchro Converter Card



Description

The The BBG-520 is a full-size ISA bus card which accommodates up to six channels of synchro/resolver output using industry standard components. Outputs are programmable synchro or resolver and can be combined with external transformers and amplifiers to supply any desired amplitude and frequency.

An DAS is available in rugged EMI/EMC enclosures.

Applications

- Radar Systems (antenna azimuth)
- Navigation Systems (gyrocompass, speedlog, course, pitch, and roll)
- Industrial Processes (position, velocity)
- Meteorology Instruments (wind speed and direction)
- Many Others

Features

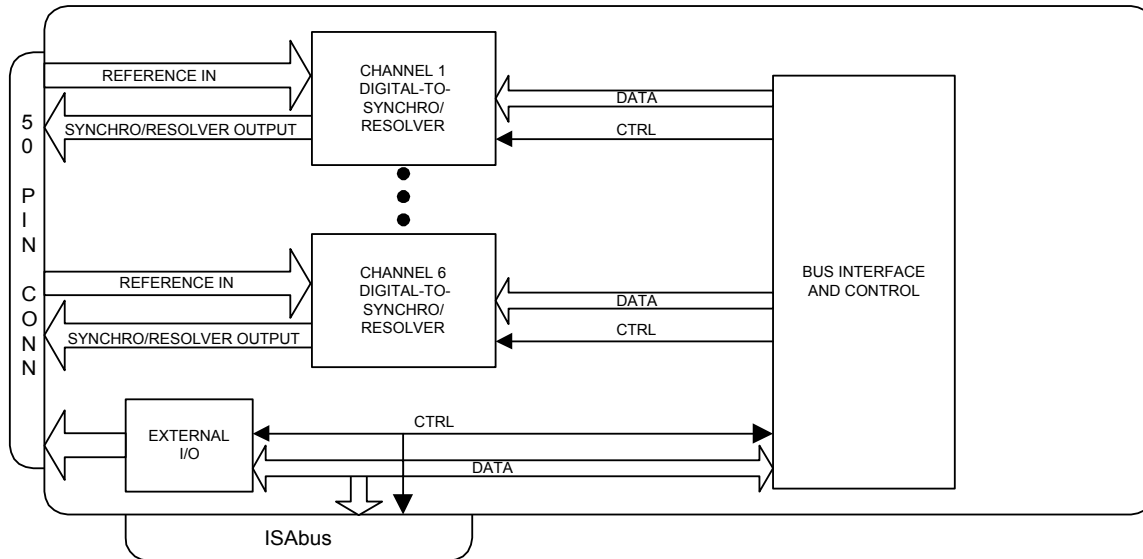
- ISAbus COMPATIBLE
- 1 TO 6 SYNCHRO/RESOLVER OUTPUTS
- JUMPER CONFIGURABLE FOR SYNCHRO OR RESOLVER OUTPUTS
- COMPATIBLE WITH SBA SERIES FOR HIGH POWER OUTPUT
- UP TO 2VA OUTPUT WITHOUT USING SBA

BBG Incorporated

1708 South Park Court • Chesapeake, VA 23320

Phone:(757) 366-9211 • Fax:(757) 366-9170 • E-mail: sales@bbginc.com • Website: www.bbginc.com

Chart



The BBG-520 is capable of interfacing to six synchro/resolver and eight digital interfaces.

Technical Specifications

Parameter	Value	Units
Power Supply *	5	Volts
	590	MiliAmps
Temperature Range		
	Operating	0 to +50
Storage	-65 to +150	C°
Input/Output		
Synchro	90 and 11.8	Volts
	0-2000	Hertz
Resolver	6.8	Volts
	0-2000	Hertz
Digital	8 bit	TTL
	5	Vdc
Dimensions	4.5 x 13.5 x 0.6	in
	11.4 x 34.3 x 1.5	cm

Table 2. BBG-520 Technical Specifications

* Power requirements depend on configuration. See converter data sheets for power requirements. External +15V and -15V supplies required for 1.5VA and 2VA outputs.



1708 South Park Court • Chesapeake, VA 23320
 Phone: (757) 366-9211 • Fax: (757) 366-9170
 E-mail: sales@bbginc.com • Website: www.bbginc.com

OVERVIEW

The BBG-520 is a full-size ISA bus card which accommodates up to six channels of synchro/resolver output using industry standard components. Outputs are programmable synchro or resolver and can be combined with external transformers and amplifiers to supply any desired amplitude and frequency.

The BBG-520 provides a status register and 12 bits of external I/O. Software drivers allow easy integration into a PC compatible computer.

SOFTWARE

The BBG-520 is shipped with a software checkout program (SAMPLE.EXE) as well as software drivers written in C (DRIVER.C) and ADA (DRIVER.ADA). These programs contain the function calls needed to operate the pc interface and convert the floating point angle to the proper format to be sent to the converter chips. This format, known as Binary Angle Measurement (BAM) is shown in Table 2

The program sample.exe (source sample.c) can be used to check out the card and serves as an example on how to use the driver programs found in DRIVER.C and DRIVER.ADA.

BINARY ANGLE MEASUREMENT FORMAT		
BIT	DEG/BIT	MIN/BIT
1 (MSB)	180	10,800
2	90	5,400
3	45	2,700
4	22.5	1,350
5	11.25	675
6	5.625	337.5
7	2.813	168.75
8	1.405	84.38
9	0.7031	42.19
10	0.3516	21.09
11	0.1758	10.55
12	0.0879	5.27
13	0.0439	2.64
14	0.0220	1.32
15	0.0110	0.66
16	0.0055	0.33

Table 2. BINARY ANGLE MEASUREMENT FORMAT

SELECTING AN ADDRESS

The BBG-520 uses sixteen (16) I/O addresses. The six converters require twelve addresses, two per converter. The bit and external ports take up four addresses. This block of addresses can be placed in memory using the three on board hex switches.

The base address of the card is set by switches SW1, SW2, and SW3. SW1 sets address bits 15-12, SW2 sets address bits 11-8, and SW3 sets address bits 7-4. This allows the card to be placed on any 16 bit boundary in I/O space.

Examples of switch positions and card addresses follow with an I/O map of the card shown in Table 4.

Example: SW1 is set to 0, SW2 is set to 3, and SW3 is set to 0.
The address of the card is 300-30F. (Factory Default)

Example: SW1 is set to 0, SW2 is set to 3, and SW3 is set to 2.
The address of the card is 320-32F.

BBG-520 I/O ADDRESS MAP			
ADDRESS	REGISTER	ADDRESS	REGISTER
XXX0	Conv 1 LOW	XXX8	Conv 5 LOW
XXX1	Conv 1 HIGH	XXX9	Conv 5 HIGH
XXX2	Conv 2 LOW	XXXA	Conv 6 LOW
XXX3	Conv 2 HIGH	XXXB	Conv 6 HIGH
XXX4	Conv 3 LOW	XXXC	Port A
XXX5	Conv 3 HIGH	XXXD	Status Port
XXX6	Conv 4 LOW	XXXE	Port C
XXX7	Conv 4 HIGH	XXXF	Port Control

Table 4. BBG-520 I/O Address Map

PARALLEL PORT

The BBG-520 uses a standard 8255 Programmable Peripheral Interface. Port B of the 8255 are status inputs from each converter. Port A is an 8 bit port connected directly to the 50 pin D connector. The upper 4 bits of port C are also connected to the 50 pin connector. Port C bits 0 and 1 and Port B bits 7 and 6 are connected to wire wrap pins on the PC card.

Ports A and C can be programmed as inputs or outputs and can be used together to control a printer or data logger.

OPTIONS

OPTION 11520 or 11524

When using the 11520 or 11524 option, the BBG-520 can be field configured for 11.8Vrms synchro or 6.8Vrms resolver outputs. Custom voltages and frequencies are available upon request. Please specify desired voltage when ordering card.

CONFIGURATION JUMPER LIST

OUTPUT: 11.8 Vrms L-L SYNCHRO MODE						
Channel	1	2	3	4	5	6
JUMPERS	P1 1 - 2	P5 1 - 2	P9 1 - 2	P13 1 - 2	P17 1 - 2	P21 1 - 2
	3 - 4	3 - 4	3 - 4	3 - 4	3 - 4	3 - 4
	P2 1 - 2	P6 1 - 2	P10 1 - 2	P14 1 - 2	P18 1 - 2	P22 1 - 2

Table 5. BBG-520 11.8 Vrms Synchro Jumper List

OUTPUT: 6.8 Vrms L-L RESOLVER MODE						
Channel	1	2	3	4	5	6
JUMPERS	P1 2 - 3	P5 2 - 3	P9 2 - 3	P13 2 - 3	P17 2 - 3	P21 2 - 3
	5 - 6	5 - 6	5 - 6	5 - 6	5 - 6	5 - 6
	P2 NONE	P6 NONE	P10 NONE	P14 NONE	P18 NONE	P22 NONE

Table 6. BBG-520 6.8 Vrms Resolver Jumper List

INPUT: 26 Vrms DC to 1000 Hz (to 10kHz reduced accuracy)						
Channel	1	2	3	4	5	6
JUMPERS	P3 1 - 2	P7 1 - 2	P11 1 - 2	P15 1 - 2	P19 1 - 2	P23 1 - 2
	P4 1 - 2	P8 1 - 2	P12 1 - 2	P16 1 - 2	P20 1 - 2	P24 1 - 2
	No Resistors in R1 - R12					

Table 7. BBG-520 Reference Input Jumper List

INPUT: Other than 26 Vrms, DC to 1000 Hz						
Channel	1	2	3	4	5	6
JUMPERS	P3 NONE	P7 NONE	P11 NONE	P15 NONE	P19 NONE	P223 NONE
	P4 NONE	P8 NONE	P12 NONE	P16 NONE	P20 NONE	P24 NONE
	* R1 * R2	* R3 * R4	* R5 * R6	* R7 * R8	* R9 * R10	* R11 * R12

Table 8. BBG-520 Reference Input Jumper List

* Resistor values are determined by the following calculation:

$$R = (5000/1.3)(V_{ref}-1.3)(\text{Nominal L-L voltage desired}/\text{Desired L-L voltage level})$$

OHMS

where V_{ref} = Reference Voltage Level

Nominal L-L voltage level = 6.81v RESOLVER or 11.8v SYNCHRO

Desired L-L voltage level must be less than or equal to the Nominal voltage level.

R is in ohms.

example: if V_{ref} = 26 Vrms

Nominal L-L voltage = 11.8V p-p

Desired L-L voltage = 10Vrms

then $R = (5000/1.3)(26-1.3)(11.8/10)$ or 112.1 K ohms.

OPTION 10520

When using the 10520 option, the BBG-520 operates at up to 2 VA at 6.8Vrms resolver outputs. Custom voltages and frequencies are available upon request. Please specify desired voltage when ordering card. External power supplies are required to operate the 2VA converters.

CONFIGURATION JUMPER LIST

OUTPUT: 6.8 Vrms L-L RESOLVER MODE						
Channel	1	2	3	4	5	6
JUMPERS	P1 2-3 6-7	P5 2-3 6-7	P9 2-3 6-7	P13 2-3 6-7	P17 2-3 6-7	P21 2-3 6-7
	P2 NONE	P6 NONE	P10 NONE	P14 NONE	P18 NONE	P22 NONE

Table 9. BBG-520 6.8 Vrms Resolver Jumper List

INPUT: 3.4 Vrms and larger DC to 1000 Hz						
Channel	1	2	3	4	5	6
JUMPERS	P3 NONE	P7 NONE	P11 NONE	P15 NONE	P19 NONE	P23 NONE
	P4 NONE	P8 NONE	P12 NONE	P16 NONE	P20 NONE	P24 NONE
	* R1 * R2	* R3 * R4	* R5 * R6	* R7 * R8	* R9 * R10	* R11 * R12

Table 10. BBG-520 Reference Input Jumper List

* Resistor values are determined by the following calculation:

$$R = (V_{ref}-3.4)(13000)/3.4 \text{ ohms}$$

where V_{ref} = Reference Voltage Level

example: if V_{ref} = 3.4 Vrms, then $R=0$ or short wire.

$$\begin{aligned} \text{if } V_{ref} &= 26 \text{ Vrms, then } R = (26-3.4)(13000)/3.4 \\ &= 86.4 \text{ kohms} \end{aligned}$$

CONNECTOR LIST FOR BBG-520

I/O CONNECTOR TYPE: DD50PA

CONNECTOR MATE: DD50S

PIN NO	SIGNAL	PIN NO	SIGNAL
1	S3_1/+SIN_1 (OUTPUT)	26	RH5 (INPUT)
2	S2_1/-COS_1 (OUTPUT)	27	RL5 (INPUT)
3	S1_1/CHAN 1 RTN (OUTPUT)	28	S3_6/+SIN_6 (OUTPUT)
4	RH1 (INPUT)	29	S2_6/-COS_6 (OUTPUT)
5	RL1 (INPUT)	30	S1_6/CHAN 6 RTN (OUTPUT)
6	S3_2/+SIN_2 (OUTPUT)	31	RH6 (INPUT)
7	S2_2/-COS_2 (OUTPUT)	32	RL6 (INPUT)
8	S1_2/CHAN 2 RTN (OUTPUT)	33	-Vext (INPUT) *
9	RH2 (INPUT)	34	+5V (IN/OUT)
10	RL2 (INPUT)	35	+5V (IN/OUT)
11	S3_3/+SIN_3 (OUTPUT)	36	GND
12	S2_3/-COS_3 (OUTPUT)	37	GND
13	S1_3/CHAN 3 RTN (OUTPUT)	38	XCD7 (INPUT/OUTPUT)
14	RH3 (INPUT)	39	XCD6 (INPUT/OUTPUT)
15	RL3 (INPUT)	40	XCD5 (INPUT/OUTPUT)
16	+Vext (INPUT) *	41	XCD8 (INPUT/OUTPUT)
17	+Vext (INPUT) *	42	XAD7 (INPUT/OUTPUT)
18	S3_4/+SIN_4 (OUTPUT)	43	XAD6 (INPUT/OUTPUT)
19	S2_4/-COS_4 (OUTPUT)	44	XAD5 (INPUT/OUTPUT)
20	S1_4/CHAN 4 RTN (OUTPUT)	45	XAD4 (INPUT/OUTPUT)
21	RH4 (INPUT)	46	XAD3 (INPUT/OUTPUT)
22	RL4 (INPUT)	47	XAD2 (INPUT/OUTPUT)
23	S3_5/+SIN_5 (OUTPUT)	48	XAD1 (INPUT/OUTPUT)
24	S2_5/-COS_5 (OUTPUT)	49	XAD0 (INPUT/OUTPUT)
25	S1_5/CHAN 5 RTN (OUTPUT)	50	-Vext (INPUT) *

* NOTE: +Vext and -Vext are required when using 10520 option. Connect external power as follows:

+15V DC, +/- 5%

connect to 50 pin D connector J2 pins 16 and 17

-15V DC, +/- 5%

connect to 50 pin D connector J2 pins 16 and 17

DC RETURN

connect to 50 pin D connector J2 pins 36 and 37